## ABSTRACT OF THE DISCLOSURE

Disclosed is a video signal processing apparatus comprising a plurality of line memories to which in sequence input video signal data is written on a line-by-line basis; a timing controller for controlling a timing to write video signal data to the plurality of line memories and a timing to read video signal data from the plurality of line memories; a computation output portion for computing video signal data read from the plurality of line memories and outputting video signal data differing in resolution which is determined by a pixel count in the horizontal direction and a line count in the vertical direction; and a line controller which vary the pixel count in specified lines of video signal data obtained from the computation output portion, depending on a conversion rate of the video signal data resolution.